Active Power Filters for Line Conditioning: A Critical Evaluation

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Abstract—**This paper presents a critical analysis of various topologies for power circuits used in power line conditioners designed to attenuate or remove disturbances in the electric power system. By defining a series of merit figures, it becomes possible to appraise the desirable qualities shown by the technical and economical aspects in each configuration. There is also a description of the basic lines for designing practical equipment. Finally, experimental results of a novel topology which reconfigurates to UPS operation in the case of a power line failure are shown to confirm the validity of the prospective method.**

Index Terms—**Active power filter, active power line conditioner, harmonic distortion, power quality.**

I. INTRODUCTION

IT IS of interest to have power line conditioners based on active power filters that are capable of attenuating disturbances, so that they can be installed on low voltage outlets from transformer stations or at the input to customer installations, wherever the network quality is below the required standard. A review of its present situation and its future prospects can be found in [5], [6], and [8]. It can be deduced, from the description of equipment for enhancing network quality which is given in those references, that uninterruptible power supplies (UPS) provide a technically optimum solution concerning the quality supplied to the load which they feed. In the search for better cost effectiveness, equipment known as power line conditioners, network conditioners or simply conditioners have been researched and developed. Such equipment provides normally a slightly lower standard in the power quality that is supplied, but they also allow a significant cost reduction and, in the more comprehensive versions, a better solution with respect to disturbances introduced into the network.

II. SPECIFICATIONS AND MERIT FIGURES

A. Specifications

The input and output specifications for a generic conditioner having a capability to compensate voltage and current are given hereunder. The following figures have been chosen for calculating power circuit components in topologies that will be discussed in the following section.

1) Input Characteristics:

Rated voltage and frequency	220/380 V, 50 Hz
Input voltage tolerance limits	±18%
Input current distortion at 20% (power) typical nonlinear load, as defined in Fig. 1	6% total, 4% at any harmonic

2) Output Characteristics:

Nominal power is in the range	25-1000 kVA
Voltage static stability	±3%
Output voltage total harmonic distortion at linear load and input voltage with less than 5% distortion	≤2%
Reactive power compensating capacity (inductive and capacitive)	25% of rated power
Mains total failure compensation capacity	500 ms, with 20% rated power

B. Comparative Evaluation Criteria

It is intended to perform a comparative technical and economical evaluation of the topologies which are described in the following section. Several technical-economical aspects have been chosen which will be quantified using the coefficients defined below.

1) Semiconductor Usage Coefficient: It is defined as the ratio of the equipment rated output power (S_n) and the sum of RMS current × RMS voltage products referred to all switches.

Bearing in mind the range of power ratings of the equipment covered by this work, electronic switches that form part of the topologies in question must be constructed using IGBT or MOSFET type switching devices and diodes. The cost difference between the transistor and the diode, when they form part of a specific switch configuration, is taken into account by the weighted sum thereof. Here, these costs are estimated in a proportion of 4 : 1 (transistor : diode). The aforegoing justifies the expression to be used for finding the usage coefficient, which is:

$$C_{aS} = \frac{S_n}{\sum_{j=1}^{N_S} \left(n_{TRj} + \frac{n_{Dj}}{4} \right) \frac{U_{Sj}}{\sqrt{2}} \frac{I_{Sj}}{\sqrt{2}}}$$

$$= \frac{S_n}{\sum_{j=1}^{N_S} \left(n_{TRj} + \frac{n_{Dj}}{4} \right) \frac{\hat{U}_{Sj}\hat{I}_{Sj}}{2}} \tag{1}$$
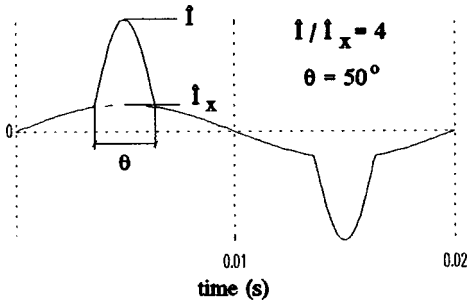
Fig. 1. Typical nonlinear load current waveform.

where S_n is the equipment output apparent power rating; N_S is the total number of switches in the topology in question, n_{TRj} is the number of switching transistors which compose, associated in parallel or in series, the electronic switch j; n_{Dj} is the number of diodes, which compose, associated in parallel or in series, the electronic switch j; U_{sj} and $\hat{U}_{sj}$ are the RMS and maximum peak voltage in every transistor and diode in switch j, respectively; I_{sj} and $\hat{I}_{sj}$ are the RMS and the maximum peak current in every transistor and diode in switch j, respectively. It is supposed that the peak voltage and the peak current in the transistors and in the diodes which compose an electronic switch are equal.

2) Coil and Transformer Usage Coefficient: The usage coefficient for coils and transformers is defined as the ratio between the equipment output rated power (S_n) and the sum of the *equivalent 50 Hz powers ($S^*_{L\text{-}TR}$)* of coils and transformers. That is to say, for a topology having $N_{L\text{-}TR}$ electromagnetic components:

$$C_{aL\text{-}TR} = \frac{S_n}{\displaystyle\sum_{j=1}^{N_{L\text{-}TR}} S^*_{L\text{-}TRj}}. \tag{2}$$

Equivalent 50 Hz power of an electromagnetic component is defined as the power rating of the simple isolating transformer for 50 Hz and sinusoidal waveform, working under typical magnetic, electric and thermal conditions, that could be constructed using the same core and copper that would be needed to make this component for its specified working conditions. The *equivalent 50 Hz power* rating derives from the *effective power* concept by adding manufacturing and economical weighting. It allows to update the price of the electromagnetic component in question from an up-to-date price list for commercial 50 Hz transformers. The following expression is used to find the *equivalent 50 Hz power ($S^*_{L\text{-}TR}$)* of an electromagnetic component having N_w windings which handle RMS voltage and current values U_k and I_k ($k = 1, \cdots, N_w$):

$$S^*_{L\text{-}TR} = F_{L\text{-}TR} \tfrac{1}{2} \sum_{k=1}^{N_w} U_k I_k \tag{3}$$

where $F_{L\text{-}TR}$ is the correction factor to take into account the difference between the component operating conditions and the standard operating conditions. Due to high switching frequencies, in the topologies treated here, air core inductors are used

to limit losses. For an inductance value, an air core inductor requires more turns (and consequently its cost is higher) than an iron core inductor. The estimated additional cost is 30% and therefore the correction factor will be 1.3 in this case.

3) Capacitor Usage Coefficient: The capacitor usage coefficient is defined as the ratio of the equipment output apparent rated power (S_n) to the sum of capacitor *equivalent 50 Hz power ratings (S^*_C)*. That is to say, for a topology having N_C capacitors:

$$C_{aC} = \frac{S_n}{\displaystyle\sum_{j=1}^{N_C} S^*_{Cj}}. \tag{4}$$

In the same way as was stated above for the *equivalent 50 Hz power rating* in electromagnetic components, the following definition is proposed for capacitors: *capacitor equivalent 50 Hz power rating* is the reactive power rating for a 50 Hz ac capacitor that has the same cost as the capacitor in question. This figure allows easily to obtain an updated price for the capacitor in question from an up-to-date price list of common 50 Hz ac capacitors. The following equations are proposed in order to find these power rating, depending upon whether the capacitor in question is ac or dc:

a) For ac capacitors

$$S^*_C = 2\pi 50 C U_C^2 \left(1 + \frac{f_C - 50}{5000}\right) \tag{5}$$

where f_C is the operating frequency, C is the capacitance, and U_C is the RMS voltage rating across its terminals. The enclosed expression takes into account the typical cost difference between one capacitor for 50 Hz and one capacitor for frequency f_C.

b) For dc capacitors

$$S^*_C = F_C U_{C=} I_{C,\sim 2} \tag{6}$$

where $U_{C=}$ is the dc voltage rating across its terminals, and $I_{C,\sim 2}$ is the RMS value of the equivalent alternating current component at 100 Hz for the current flowing through it. F_C is a correction factor which accounts for the difference in cost between a dc capacitor (electrolytic capacitor), and an ac capacitor having the same apparent power rating (where, for dc capacitors, such power rating is taken as the product $U_{C=} I_{C,\sim 2}$). An acceptable value for F_C obtained from practical considerations is 0.25 or similar.

A more detailed description and application of these merit figures can be found in [16].

III. COMPARATIVE ANALYSIS

Once classification work had been completed and the general specifications established, a detailed study was conducted on the most significant single phase topologies. Their power circuit design calculations were developed to make them fulfill the proposed specifications, and the specified usage coefficient values were calculated. A summary of this study is given below.

A. Initial Assumptions

All the equipment dealt with can be included within the family of high frequency active filter line conditioners using pulse width modulation (PWM) (taking this modulation technique in its widest sense).

In the majority of cases, voltage and current harmonics contained in the mains voltage are significant up to the seventh order. Allowing a safety margin, the compensation is suitable up to the eleventh harmonic. From this, it is seen to be advisable for the switching frequency to be 5 kHz at the very least (10×11 harmonics $\times$ 50 Hz). Given the present state of semiconductor technology and the capabilities of control systems, the proper value for the above mentioned switching frequency would be 10 kHz, and this figure will be used here as a basis in making the comparative evaluation of the various topologies.

The following operating assumptions are made in connection with the components:

1) Coils and capacitors are ideal.
2) Switching devices for the power range under consideration will be the MOSFET or the IGBT type.
3) The efficiency and voltage drop, under rated load, for transformers are 95 and 1%, respectively.

B. Power Circuit Topologies

The figure on the first column of Table I shows the half-bridge version of *Topology I1* which is described in [2], [3], and [10]. The equipment covered in these references, and indeed the majority of present day current conditioners, are able to compensate harmonics and reactive current, but they are not designed to compensate mains failures lasting about 0.5 s. In this work this latter specification is considered, and this is a novel contribution. This feature is obtained by feeding the critical load in the event of mains failure, from the dc busbars, at the expense of energy stored in the dc capacitors, and making the current filter converter work as an inverter after changing its control program. This mode of operation requires the network (whose voltage drops below the established limits) and the noncritical load to be isolated. Static switches SS1 and SS2 are needed for this purpose.

The power *Topology I2* is shown in the second column of Table I. Its analysis is based upon studies made in [4] and [9]. In the same manner as with Topology I1, and for the same reasons as are mentioned there, the survey being conducted here covers the compensation capacity for mains failures lasting one half second. This comprises a novel contribution. When this feature is incorporated, static switches SSI and SS2 have to be included.

Topology U1 is a voltage active filter topology, with a compensator transformer that is fed by an ac/ac converter. This configuration (see [1]) allows currents handled by the electronic converter to be reduced in the same proportion as the transformer ratio. The figure on the third column of Table I shows the bridge version with four switches that are bidirectional in voltage and current. Filter L_2–C_2 reduces voltage harmonics generated by the converter. The input filter L_1–C_1, will reduce harmonics in the current demanded from the mains, and will attenuate noise and pulses in differential mode.

Power Circuit *Topology U2* is a topology that has a compensated transformer fed by an ac/dc/ac converter. Generally speaking (see [7]), it follows that of the classic stabilizers with compensating transformers. The figure on the fourth column of Table I illustrates this topology with the half-bridge/half-bridge version. The *ac/dc converter* is a *synchronous rectifier* that is provided with pulse width modulation (PWM) control. The *dc/ac converter* is a voltage source inverter and is likewise provided with pulse width modulation (PWM) control. Its output voltage (u_{BO}) is filtered by the second order low-pass filter L_2–C_2. This voltage, whose value is controllable, is added to the input voltage through the compensator transformer.

The structure of Power Circuit *Topology UI* is shown in the fifth column of Table I. It can be regarded as the association of a current conditioner Topology I1, and a voltage compensator with the dc to ac circuit of Topology U2. They are linked through the dc voltage busbars, U_{dc}. The compensating transformer is connected in series with one of the mains wires. The current section terminals are connected in parallel with the load. With this arrangement, harmonic currents demanded by the nonlinear load do not flow through the compensating transformer.

A similar topology is analyzed in [13]. The one described here is different as it provides with an increased size of capacitive energy storage (about five times the value needed by ripple considerations) to compensate mains failures lasting one half second. Due to the same reasons as for Topology I1, the incorporation of this characteristic makes it necessary to include static input and output switches SS1 and SS2.
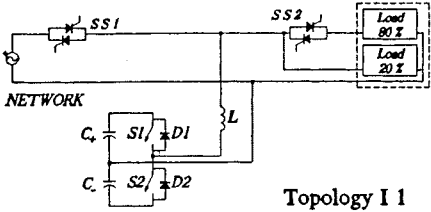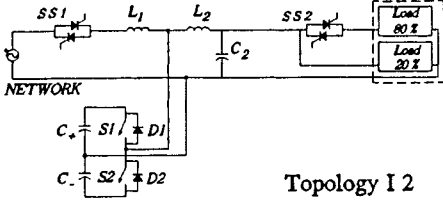
C. Comparative Evaluation

By applying the merit figures defined above, it becomes possible to make a comparative evaluation of the topologies that have been examined. Table I shows a summary for each topology, including their basic compensation characteristics, their design data and the findings obtained for their usage coefficients as calculated in accordance with their definition.

The advantages predicted by the comparative evaluation for Topology UI have been exhaustively investigated and checked by means of the 3 kVA and the 400 kVA prototypes described in Section IV. The results reveal that this topology is a good choice for a universal line conditioners including UPS operation [11].

IV. EXPERIMENTAL PROTOTYPES

The above study has been tested in several protypes. The main one is a research project, [12], [15], which includes work on developing a voltage and current conditioner (Topology UI) by applying in practice a 3 kVA three phase laboratory prototype, and a three phase industrial prototype rated at 400 kVA for a 220/380 V line. The basic compensation characteristics of the equipment are shown by the waveforms in Figs. 2 and 3. The control circuit has two interactive processors, one for the voltage filter and another for the current filter. Both processors operate under a deadbeat technique (see [11] for a comprehensive description). In the voltage section control circuit network voltage and load current are the input signals and the output is the duty cycle for switches. This signal is applied to a pulse pattern generator

TABLE I
COMPARISON OF FIVE POWER LINE CONDITIONER TOPOLOGIES. SWITCHING FREQUENCY 10 KHz

Basic Diagram	Topology I 1	Topology I 2
* Coils	$L = 0.000695\ U_n^2/S_n$ $I_L = 0.27\ I_n$ $S^*_L = 0.010\ S_n$	$L_1 = 0.000695\ U_n^2/S_n$ $I_{L1} = I_n$ $S^*_{L1} = 0.1335\ S_n$ $L_2 = 0.0002\ U_n^2/S_n$ $I_{L2} = I_n$ $S^*_{L2} = 0.0408\ S_n$
* Capacitors	$C = 0.0354\ S_n/U_n^2$ $U_{C=} = 1.83\ U_n$ $I_{C.\sim 2} = 0.19\ I_n$ $S^*_C = 0.087\ S_n$	$C_2 = 0.0002\ U_n^2/S_n$ $U_{C2} = U_n$ $f_C = 10$ kHz $S^*_{C2} = 0.1884\ S_n$ $C_+ = C_- = 0.0354\ S_n/U_n^2$ $U_{C=} = 1.83\ U_n$ $I_{C.\sim 2} = 0.19\ I_n$ $S^*_C = 0.087\ S_n$
* Transformers		
* Semiconductors	$\hat{U}_S = 3.67\ U_n$ Converter $\hat{I}_S = 0.36\ I_n$ Switches $\hat{U}_S = 1.67\ U_n$ Input $\hat{I}_S = 1.41\ I_n$ Switch (SS1) $\hat{U}_S = 1.67\ U_n$ Output $\hat{I}_S = 1.13\ I_n$ Switch (SS2)	$\hat{U}_S = 3.67\ U_n$ Converter $\hat{I}_S = 0.36\ I_n$ Switches $\hat{U}_S = 1.67\ U_n$ Input $\hat{I}_S = 1.41\ I_n$ Switch (SS1) $\hat{U}_S = 1.67\ U_n$ Output $\hat{I}_S = 1.13\ I_n$ Switch (SS2)
Usage Coefficients * Coils and Transformers ($C_{aL\text{-}TR}$) * Capacitors (C_{aC}) * Semiconductors (C_{aS})	100 5.74 0.14	5.72 2.76 0.14
Voltage Specifications * Input Voltage Margins: $\pm$ 18 % * Output Voltage Static Stability: $\pm$ 3	NO	NO
Current Specifications * Imput current THD < 6% with typical non-linear load * Reactive Power Conpensating Capacity: 25 % of Rated Power	YES	YES
Outage Compensation $\leq$ 500 ms	YES	YES

U_n : Equipment Rated Voltage (RMS)

S_n : Equipment Apparent Rated Power

$S^*_L \cdot S^*_{TC}$: *Equivalent 50 Hz Power* for a Coil or Transformer
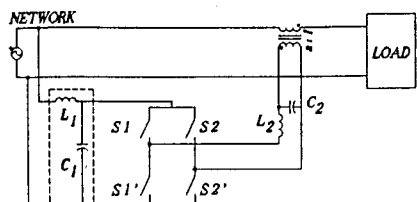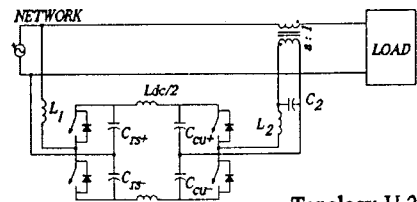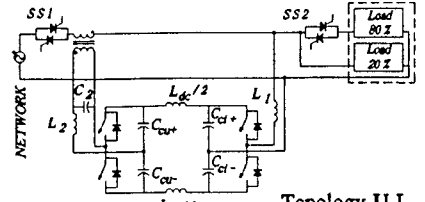
U_C : A.C. Capacitor Rated Voltage (RMS)

I_n : Equipment Rated Current (RMS)

S^*_C : Capacitor *Equivalent 50 Hz Power*

I_L : Coil Rated Current (RMS)

$U_{C=}$: D.C. Capacitor Rated Voltage

Topology U 1	Topology U 2	Topology U I
$L_1 = 0.00328\ U_n^2/S_n$ $I_{L1} = 0.2\ I_n$ $S^\bullet_{L1} = 0.0291\ S_n$	$L_1 = 0.000695\ U_n^2/S_n$ $I_L = 0.2\ I_n$ $S^\bullet_{L1} = 0.0058\ S_n$	$L_1 = 0.000695\ U_n^2/S_n$ $I_L = 0.3\ I_n$ $S^\bullet_{L1} = 0.0132\ S_n$
$L_2 = 0.00026\ U_n^2/S_n$ $I_{L1} = 0.2\ I_n$ $S^\bullet_{L2} = 0.0023\ S_n$	$L_2 = 0.0014\ U_n^2/S_n$ $I_L = 0.12\ I_n$ $S^\bullet_{L2} = 0.0045\ S_n$	$L_2 = 0.0014\ U_n^2/S_n$ $I_L = 0.12\ I_n$ $S^\bullet_{L2} = 0.0045\ S_n$
	$L_{dc} = 0.026\ U_n^2/S_n$ $I_L = 0.1\ I_n$ $S^\bullet_{Ldc} = 0.0409\ S_n$	$L_{dc} = 0.0027\ U_n^2/S_n$ $I_L = 0.1\ I_n$ $S^\bullet_{Ldc} = 0.0042\ S_n$
$C_1 = 0.00014\ S_n/U_n^2$ $U_{C1} = U_n$ $f_C = 50$ Hz $S^\bullet_{C1} = 0.0295\ S_n$	$C_{rs} = 0.00185\ S_n/U_n^2$ $U_{C=} = 1.83\ U_n$ $I_{C.\sim2} = 0.1249\ I_n$ $S^\bullet_{Crs} = 0.057\ S_n$	$C_{ci} = 0.0177\ S_n/U_n^2$ $U_{C=} = 1.83\ U_n$ $I_{C.\sim2} = 0.2163\ I_n$ $S^\bullet_{Cci} = 0.0992\ S_n$
$C_2 = 0.00002\ S_n/U_n^2$ $U_{C2} = 0.75\ U_n$ $f_C = 10$ kHz $S^\bullet_{C2} = 0.0108\ S_n$	$C_2 = 0.000013\ U_n^2/S_n$ $U_C = 1.28\ U_n$ $f_C = 10$ kHz $S^\bullet_{C2} = 0.0609\ S_n$	$C_2 = 0.000013\ S_n/U_n^2$ $U_C = 1.28\ I_n$ $f_C = 10$ kHz $S^\bullet_{C2} = 0.0609\ S_n$
	$C_{cu} = 0.0011\ U_n^2/S_n$ $U_{C=} = 1.83\ U_n$ $I_{C.\sim2} = 0.076$ $S^\bullet_{Ccu} = 0.035\ S_n$	$C_{cu} = 0.0177\ S_n/U_n^2$ $U_{C=} = 1.83\ U_n$ $I_{C.\sim2} = 0.076\ I_n$ $S^\bullet_{Ccu} = 0.035\ S_n$
$a = 5$ $U_{sec} = 0.15\ U_n$ $I_{sec} = I_n$ $S^\bullet_{TC} = 0.15\ S_n$	$a = 8.5$ $U_{sec} = 0.15\ U_n$ $I_{sec} = I_n$ $S^\bullet_{TC} = 0.15\ S_n$	$a = 8.5$ $U_{sec} = 0.15\ U_n$ $I_{sec} = I_n$ $S^\bullet_{TC} = 0.15\ S_n$
$\hat{U}_S = 1.668\ U_n$ $\hat{I}_S = 0.2947\ I_n$	$\hat{U}_S = 3.67\ U_n$ $\hat{I}_S = 0.2874\ I_n$ Synchronous Rectifier	$\hat{U}_S = 3.67\ U_n$ $\hat{I}_S = 0.51\ I_n$ Current Compensator
	$\hat{U}_S = 3.67\ U_n$ $\hat{I}_S = 0.1734\ I_n$ Voltage Compensator	$\hat{U}_S = 3.67\ U_n$ $\hat{I}_S = 0.1734\ I_n$ Voltage Compensator
		$\hat{U}_S = 1.67\ U_n$ $\hat{I}_S = 1.41\ I_n$ Input Switch (SS1)
		$\hat{U}_S = 1.45\ U_n$ $\hat{I}_S = 1.13\ I_n$ Output Switch (SS2)
5.5 24.8 0.5	4.97 4.08 0.47	5.8 3.03 0.12
YES	YES	YES
NO	NO	YES
NO	NO	YES

$I_{C,\sim2}$: Equivalent a.c. component at 100 Hz (RMS) for the current flowing through a d.c. capacitor.

I_{sec} : Transformer Secondary Rated Current (RMS) f_C : Rated Working Frecuency for a a.c. Capacitor

U_{sec} : Transformer Secondary Rated Voltage (RMS) a : Transformer Ratio

$\hat{I}_S$: Maximun Peak Current in a Switch $\hat{U}_S$: Maximun Peak Voltage in a Switch
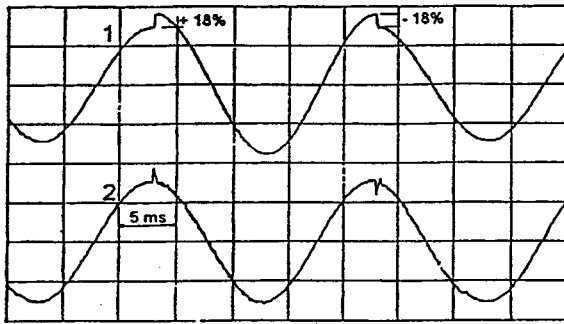
Fig. 2. Experimental results (Topology UI). Compensation of two +18 and −18% consecutive steps in mains voltage.
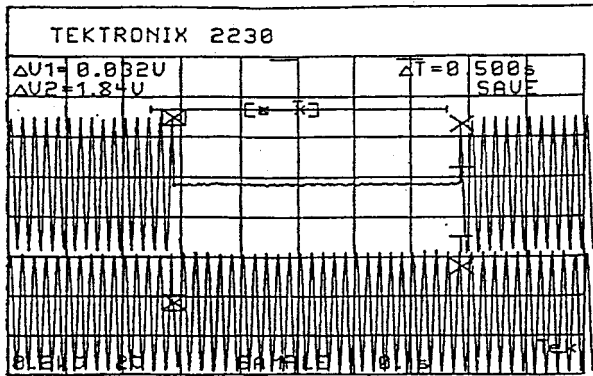

Fig. 3. Experimental results for voltage and current conditioner (Topology UI). UPS operation during a 500 ms line outage.

which drives the electronic switches. The current section control circuit senses the load current and generates the appropiate trigger gate signals. This power topology needs at least an additional control loop to maintain the dc link voltage within certain limits.

V. CONCLUSIONS

In-depth cost-effective comparative analysis of a number of power line conditioners has been carried out. In several of them certain novel modifications have been made in a previous electronic study in search of a reconfigurable topology to UPS. Several merit figures have been developed for the purpose of making a critical economic evaluation of these topologies. These figures can be used for making technical and cost appraisals of power conditioner equipment in general. Three prototypes of 1, 3, and 400 kVA of the Topology UI have been tested. The experimental results summarized in Figs. 2 and 3 confirms a fast response time and the ability to eliminate short line outages for this cost-effective topology, economically prevalidated by the proposed prospective method and merit figures.

It is important to note that, when applying this comparative study to the detailed design of a specific line conditioner, small corrections of the merit coefficients must be made taking into account the particular control strategy adopted. In any case, this study should be of great help to the designer, in as much that it will provide him with the initial basic ideas and comparative figures required when making a practical design.

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