Power Injection System for Photovoltaic Plants based on a Multiconverter Topology with DC-Link Capacitor Voltage Balancing

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Abstract—This paper presents the simulation of a new topology for the power injection system of a single-phase grid connected photovoltaic generation system that is based on the parallel association of two voltage source inverters: one is a 3 level neutral point clamped operated using a low switching frequency strategy and the other is a 2 level inverter which operates with a pulse width modulation based strategy. The aim of this topology is that multilevel inverter injects the power and the other inverter controls the current quality. The DC-link capacitor voltage balancing is solved by using the redundant states of the multilevel inverter. The proposal optimizes the system design, allowing high power injection, permitting reduction of system losses and an increase of the energy injected into the grid.

I. INTRODUCTION

The number of photovoltaic generation systems (PVGS) is increasing very fast in Spain, which is principally due to the daylight hours with an optimal irradiance and temperature and to the Spanish government subsidies.

The energy produced by a PVGS must be injected into the electric grid, according to pre-established quality and reliability specifications, without affecting grid’s normal operation. This involves a low harmonic distortion and an accurate synchronization for the current injected.

The PVGS contains a power injection system (PIS) that has the function of injecting the power produced by the photovoltaic cell groups, converting the energy from the original DC form to the final AC form with the desired electrical characteristics. The part of the PIS that carries out this conversion is the inverter [1][2]. Usually, Pulse Width Modulation (PWM) based inverters [1][3] or multilevel topology inverters are used [1][4].

In this paper a new topology for the PIS based on the parallel association of two voltage source inverters (VSI) is presented and analyzed by means of simulation. The first one is a single-phase 3 level neutral point clamped inverter (3-L NPC) operated using a low switching frequency quasi-square voltage waveform strategy with selective harmonic elimination (SHE) which is called quasi-square waveform multilevel inverter (QSWMI) [5][6]. The second one is a single-phase 2 level inverter operated with a PWM hysteresis band strategy which is called high-switching-frequency inverter (HSFI).

The general purpose of the QSWMI is to inject the power generated by the PVGS; while the HSFI controls the quality of the current injected into the grid. The PIS proposed is capable to inject a high amount of power due to the use of a multilevel inverter but at the same time it presents the challenge of the DC-link capacitor voltage balancing. This issue is solved by the redundant state selection (RSS) of the 3-L NPC [6]-[9].

II. PIS DESCRIPTION

The grid connected PVGS scheme analyzed is shown in Fig. 1. A direct connection to the inverters without a previous DC/DC converter has been chosen. The upper inverter in the figure is the QSWMI or inverter 1 and the lower inverter is the HSFI or inverter 2. Both inverters are connected to the grid by means of the inductances $L_1$ and $L_2$ respectively, which are divided into two to avoid short-circuits.

A. QSWMI

The objective of this inverter is to inject the energy from the PVGS into the grid. In order to achieve this, controlling the fundamental component of the inverter voltage is sufficient, under the assumption that the voltage does not present harmonics. The power generated by the PVGS $P_{PV}$, with negligible inverter losses, is equal to the power injected into the electric grid $P_S$:

$$P_{PV} = P_S = V_S I_{S_1} \cos \varphi, \quad (1)$$

where $V_S$ is the RMS supply voltage, $I_{S_1}$ the RMS fundamental supply current component, and $\varphi$ is the displacement angle between voltage and fundamental current component, which must be null for a maximum efficiency.

![Fig. 1. Proposed system scheme.](image-url)
Examining the proposed topology (Fig. 1), one has that the fundamental voltage component of the inverter 1 is:

\[ \vec{V}_{i1} = \vec{V}_S + jL_1 \omega \vec{I}_{i1}, \]

where \( \vec{I}_{i1} \) is the fundamental current component of inverter 1 which ideally should be equal to \( I_{S1}, \) \( \vec{V}_S \) is the grid voltage and \( \omega \) is the angular frequency.

The fundamental component of the current injected by the QSWMI \( i_{11} \), which is equal to fundamental component of the supply current \( I_{S1} \), is considered as the reference current \( i_{S,ref} \):

\[ i_{11} = I_{S1} = i_{S,ref}, \]

where \( I_{11}, I_{S1} \in I_{S,ref} \) are their RMS values respectively.

The RMS value of the fundamental component of the five step quasi-square voltage multilevel inverter waveform \( V_{11} \), depends on the angles \( \alpha, \beta \) and \( \gamma \) which denote the interval with maximum, middle and null output voltage level of the QSWMI respectively in a quarter cycle (see Fig. 2). The Fourier series expansion of this waveform gives the next expression for the RMS value of the QSWMI voltage.

\[ V_{1,k} = \frac{4V_{DC}}{\sqrt{2}h\pi} \sin \left( h \left( \alpha + \frac{\beta}{2} \right) \cos \left( h \frac{\beta}{2} \right) \right), \]

where \( h \) is the harmonic order and \( V_{DC} \) is the DC bus voltage.

According to (4) there are two degrees of freedom, \( \alpha \) and \( \beta \), for controlling two properties of the QSWMI voltage. One will be used to control the RMS value of the fundamental component \( V_{11} \), and the other to eliminate the triples harmonics. All the intervals or zones that meet these premises are summarized in TABLE I. In order to cover every possible value of \( V_{11} \), the waveform is degenerated into a three step quasi-square waveform out of the triple harmonic elimination resulting four different operation zones \( Z_2 \) and \( Z_3 \) and \( Z_4 \) where the triple harmonics are null and \( Z_1 \) and \( Z_4 \) where they are not (see Fig. 3). The optimal point of operation is in \( Z_3 \) when \( \alpha = 42^\circ \) because the quintuple harmonics are also zero.

Replacing (5), (6) and (7) into (2) the system has to calculate the angles in the way the TABLE II shows.

However, the control system of this multilevel inverter not only must inject the energy into the electric grid, but must also guarantee that the displacement power factor is equal to unity. This is achieved when the current injected by the inverter is

\[ i_i = \sqrt{2}I_{S1}I_{S,ref}, \]

where \( I_{S,ref} \) is a sinusoidal wave with unity amplitude and with the same frequency and phase as the supply voltage.

Equation (2) can be expressed as

\[ \vec{V}_{i1} = \vec{V}_S + I_{S1}L_1 \omega \left( j \frac{\vec{V}_S}{V_S} \right), \]

so, an unitary sinusoidal carrier at the fundamental frequency \( u_p \) (see Fig. 4(a)) can be constructed for the QSWMI modulation process.

\[ u_p = \frac{I_{S1}L_1 \omega}{\sqrt{V_S^2 + \left( I_{S1}L_1 \omega \right)^2}} \]

where \( u_{S,ref} \) is an unitary sinusoidal wave in quadrature with respect to \( u_{S,ref} \). The carrier waveform guarantees that the quasi-square waveform maintains the phase needed to generate the fundamental supply current component in phase with the grid voltage.

Four constant waveforms are used as modulators, two for each branch of the single-phase multilevel inverter (as shown in Fig. 4(a)).

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**TABLE I**

<table>
<thead>
<tr>
<th>Waveform</th>
<th>( V_{1,k} ) (V)</th>
<th>Zones</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.45( V_{DC} ) sin ( \beta )</td>
<td>0 \leq \beta &lt; \frac{\pi}{3}</td>
<td>( Z_1 )</td>
</tr>
<tr>
<td>0.78( V_{DC} ) sin ( \beta + \frac{\pi}{6} )</td>
<td>( \frac{\pi}{6} \leq \beta &lt; \frac{2\pi}{3} )</td>
<td>( Z_2 )</td>
</tr>
<tr>
<td>0.9( V_{DC} ) sin ( \beta )</td>
<td>( \frac{\pi}{3} \leq \beta &lt; \frac{\pi}{2} )</td>
<td>( Z_4 )</td>
</tr>
</tbody>
</table>
In order to guarantee the RMS value of the fundamental supply current component, the duty cycles and the modulator waves are

\[ D_{12} = u_{M,1a2+} = -u_{M,1b2+} = \cos \alpha \]
\[ D_{1} = u_{M,1a1+} = -u_{M,1b1+} = \cos(\alpha + \beta). \] (14)

The initial switching signals for the multilevel inverter (without RSS) \( s^*_{1a2}, s^*_{1a1}, s^*_{1b2} \) and \( s^*_{1b1} \) are shown in Fig. 4(b) and Fig. 4(c). They are generated by comparing the modulators with the carrier.

\[
\begin{align*}
    s^*_{1a2} &= \begin{cases} 
    1 & \text{if } u_p < D_{12} \\
    0 & \text{if } u_p \geq D_{12}
    \end{cases} \\
    s^*_{1a1} &= \begin{cases} 
    1 & \text{if } u_p < D_{1} \\
    0 & \text{if } u_p \geq D_{1}
    \end{cases} \\
    s^*_{1b2} &= \begin{cases} 
    1 & \text{if } u_p < -D_{12} \\
    0 & \text{if } u_p \geq -D_{12}
    \end{cases} \\
    s^*_{1b1} &= \begin{cases} 
    1 & \text{if } u_p < -D_{1} \\
    0 & \text{if } u_p \geq -D_{1}
    \end{cases}
\end{align*}
\] (15)

B. HSFI

This inverter must control the quality of the current injected into the grid by adding the needed current \( (i_2) \) to the current injected by the QSWMI \( (i_1) \).

The inverter control is implemented by using a synchronous hysteresis band \([10][12]\) with a high switching frequency (usually between 10 and 20 kHz). The difference between the sinusoidal current reference \( i_{s,ref} \) and the current effectively injected into the grid \( i_s \), which equal to the sum of the currents injected from the two inverters, is used as the error signal.

\[ i_1 = i_{s,ref} - i_s. \] (16)

The operation of the hysteresis band control must eliminate the existing error so the HSFI complements the operation of the QSWMI. The switching signals for the HSFI are

\[ s^*_i = \begin{cases} 
    1 & \text{if } i_{s,ref} - i_s \geq 0 \\
    0 & \text{if } i_{s,ref} - i_s < 0
    \end{cases} \] (17)

C. Passive element selection

The QSWMI inductance value \( L_1 \) must be selected to permit the injection of the maximum power that the PVGS can generate (which depends on the irradiance \( W \) and temperature \( T \) conditions).

The power injected into the grid from the PVGS (neglecting the PIS losses) is

\[ P_{PV} = P_S = V_S i_S, \] (18)
as the current is in phase with the grid voltage.

The RMS fundamental current component injected by the QSWMI \( I_1 \) can be determined from (2):

\[ I_{1} = \frac{V_S}{2\omega L_1} \sqrt{V_{1,1}^2 - V_S^2}. \] (19)

From (18) and (19) one obtains

\[ L_1 = \frac{V_S}{2\omega P_{PV}} \sqrt{0.55V_{1,1}^2 - V_S^2}. \] (20)

From the last expression, it can be deduced the minimum DC-Link voltage by assuming a true value for \( L_1 \). The system will be designed to match the maximum power point (MPP) of the PVGS in reference operation conditions of irradiance, 1000W/m², and temperature, 25ºC, with the optimal operation point of the QSWMI which is obviously reached in \( Z_2 \), when the \( \alpha \) angle from the quasi-square waveform is 42º because the triple and the quintuple harmonics are eliminated from the voltage (and the injected current) spectrum (see Fig. 3). In addition, this consideration in design guarantees that if there is a change in the irradiance and temperature conditions, the control operation margin will be inside \( Z_2 \), where the triple harmonics are zero. Substituting (6) in (20), the inductance with the proposed DC-Link voltage \((\alpha = 42º)\) is given by

\[ L_1 = \frac{V_S}{2\omega P_{PV}} \sqrt{0.55V_{1,1}^2 - V_S^2}, \] (21)

so, for valid values, it must satisfy the following equation

\[ V_{DC} > 1.35V_S. \] (22)

The HSFI inductor \( L_1 \) must be chosen as high as possible (thus achieving maximum filtering) but taking into account that this value must permit the needed current derivatives in order to build the total supply current with the desired quality. The quality must be guaranteed even in the worst case (maximum supply voltage for the positive derivatives and
minimum for the negative ones). For a given current derivative or slope, $I_{2,\text{slope}}$, one has

$$I_2 = \frac{V_{\text{dc}} - \sqrt{2}V_s}{I_{2,\text{slope}}}. \quad (23)$$

To produce valid inductance values, one must have that

$$V_{\text{dc}} > 1.41V_s. \quad (24)$$

This condition is more restrictive for the DC-Link voltage than the one imposed by (22).

The capacitors between the PVGS and the PIS $C_1$ and $C_2$ (that ideally have the same value and are equal to $C/2$) must absorb the active power fluctuations (that always exist in a single-phase system). Therefore it achieves constant power in the output terminal of the PVGS constant under these power fluctuations.

As the supply current is in phase with the grid voltage, and assuming it to be sinusoidal, the instantaneous power becomes

$$p_{i}(t) = v_{i}(t)i_{i}(t) = 2V_is\sin^{2}\alpha \quad (25)$$

and the power fluctuations are due to the energy that is stored and discharged in the capacitor, so that the instantaneous power associated with the capacitor is

$$p_{c}(t) = p_{s}(t) - p_{PV} = p_{s}(t) - p_{i} = 2V_is\sin^{2}\alpha - V_sI_s = V_sI_s(-\cos 2\alpha). \quad (26)$$

The energy discharged from the capacitor in one quarter of the fundamental period (which will be equal to the energy stored in the next quarter) is

$$e_{c}(t) = \frac{3\sqrt{2}}{\omega} \int p_{c}(t)dt = V_sI_s \frac{3\sqrt{2}}{\omega} \left(-\cos (2\alpha)\right)dt = \frac{V_sI_s}{\omega} \left(V_sI_s\sin (2\alpha)\right) \quad (27)$$

This discharged energy produces a capacitor voltage decrease:

$$e_{c}(t) = \frac{1}{2} C \left(V_{c,\text{max}} - V_{c,\text{min}}\right) \quad (28)$$

If the voltage decrease is small, the above equation can be written as

$$e_{c}(t) = \frac{1}{2} C \left(V_{dc} + \tilde{v}_{c}\right)^{2} - \left(V_{dc} - \tilde{v}_{c}\right)^{2} = 2CV_{dc}\tilde{v}_{c} \quad (29)$$

where $\tilde{v}_{c}$ is the capacitor voltage fluctuation.

To guarantee that the relative voltage fluctuations are lower than a pre-established value, we must satisfy

$$\frac{\tilde{v}_{c}}{V_{dc}} = \frac{e_{c}(t)}{2CV_{dc}} \leq \varepsilon \Rightarrow C = 2C_1 = 2C_2 \geq \frac{p_{PV}}{2e_{dc}V_{dc}} \quad (30)$$

where $\varepsilon$ is the maximum relative value of the DC voltage ripple.

III. CAPACITORS VOLTAGE BALANCING

The capacitors voltage balancing is a problem inherent to the multilevel inverter due to the asymmetric DC-Link current flow. Obviously, it must be solved to assure that the voltage levels of the DC-Link are the desired ones. In this case, it is needed a half of the DC-Link voltage in the middle point of the DC-Link so $C_1$ must be equal to $C_2$. The best way to solve this is to take advantage of the redundant states selection RSS of the 3L-NPC which permit the same output voltages for the inverter but with a different current flow.

Looking at the proposed system scheme in Fig. 1, one can deduce that

$$v_{pv} = v_{c2} + v_{c1} \quad (31)$$

where $v_{c2}$ and $v_{c1}$ are the voltage at the capacitors $C_2$ and $C_1$ respectively, $v_{pv}$ and $i_{pv}$ are the PVGS voltage and current respectively, and $i_{dc2}$ and $i_{dc0}$ are the upper and lower DC-Link currents respectively.

To control the capacitors voltage balancing, $v_{c2}$ must be equal to $v_{c1}$. On the one side, from (31) one has that the DC-Link currents affect directly to the capacitors voltage, and from the other side one has the redundant states of the QSWMI which affects the DC-Link currents, so the control can be done by sensing the capacitors voltages and the load current and then selecting the switching state, SS, that balance the capacitors.

In the TABLE III are shown every SS of the full bridge QSWMI and its effect on the DC-Link capacitors voltages. In order to this, the control logic can be done with the redundant states: $S_1$, $S_2$, $S_3$ and $S_4$. The TABLE IV shows the selected switching state, SS, according to the control logic.

Once the SSs are calculated, it is compared with the initial switching state obtained in the QSWMI modulation process $S_1$ and results the final switching state, $S_{f}$, with the switching signals $s_{t_1}$, $s_{t_2}$, $s_{t_3}$, $s_{t_4}$, that must be applied to the inverter.

IV. CONTROL SYSTEM

The PIS control can be divided into the blocks shown in the schematic diagram of Fig. 5.

<table>
<thead>
<tr>
<th>TABLE III</th>
<th>SWITCHING STATES, OUTPUT VOLTAGES AND THEIR EFFECT ON THE DC-LINK CAPACITORS VOLTAGES</th>
</tr>
</thead>
<tbody>
<tr>
<td>$s_{t_1}$</td>
<td>$s_{t_2}$</td>
</tr>
<tr>
<td>-----------</td>
<td>-----------</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
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<tr>
<td>1</td>
<td>1</td>
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<tr>
<td>1</td>
<td>0</td>
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<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Here, “+” and “-” represent charging, discharging and no effect respectively.
A. Maximum Power Point Tracking (MPPT)

The objective of this block is to set and to maintain the PVGS at its MPP whatever the irradiance and temperature are. When the PVGS is working at this point, one has that

$$\frac{dP_{PV}}{dV_{PV}} = 0.$$  (32)

The MPPT scheme is shown in Fig. 6. In the proposed system, this condition is achieved by considering the power derivative as the error input of a proportional-integral (PI) controller. In this way if the PI controller is well designed, the power derivative will become zero in the steady state and the controller. In this way if the PI controller is well designed, the improper operation of the integral part of the controller due to the switching frequency. A low-pass filter is included to eliminate the components in the power derivative due to the start-up transients. A low-pass filter is included to eliminate the components in the power derivative due to the switching frequency.

B. Reference Supply Current Generation Block (RSCG)

This is the principal block of the proposed control system, because it guarantees that the current extracted from the PVGS is the desired one and so the MPP is tracked. The RMS value of the fundamental current component that must be injected into the grid is determined by neglecting the PIS losses:

$$I_{k,ref} = \frac{V_{PV}I_{PV,ref}}{V_g}.$$  (33)

This reference current value is tuned by the output of an additional PI whose input is the error between the reference current that must be extracted from the PVGS (determined by the MPPT block) and the actual one (measured from the system). The aim of this tuning is to compensate the system losses that have not been considered in (33).

The RSCG block contains a synchronization module [13] that generates two sinusoidal signals with unity amplitude, which are in phase ($\alpha_{a,q}$) and in quadrature ($\beta_{a,q}$) with the fundamental grid voltage component, and a RMS grid voltage fundamental component calculation module [14]-[16].

As a result the reference supply current is a sinusoidal wave ($i_{S,ref}$) in phase with the grid voltage, and its RMS value is equal to that given by (33).

The resulting diagram for this block is shown in Fig. 7.

C. Inverters Switching Signal Generation

This block implements the collaboration between the two inverters. Their principle of operation was described in section II. Fig. 8 and Fig. 9 show the schematic diagram for the QSWMI inverter and the HSFI inverter respectively.

The QSWMI is operated in a quasi-open-loop obtaining the value of $\alpha$ and $\beta$ in each operation zone from the reference supply current ($i_{S,ref}$), not its measured value. The RSS is placed here to obtain the final switching signals.

The HSFI switching signals are generated based on the error existing between the reference supply current and the measured one, by using a synchronous hysteresis band that compares the error with zero for a fixed sample period.

D. Redundant State Selection (RSS)

This block implements the redundant state selection for the QSWMI to balance the capacitors voltages. Its operation was described in section III and its block scheme is shown in Fig. 10. Basically, it takes the switching signals generated in the QSWMI modulation algorithm $SS_1$ and generates the final switching state $SS_5$ selecting the redundant states of the multilevel $SS_k$ in order to balance the DC-Link capacitors voltages (see TABLE IV).
The final switching states are obtained with a look up table LUT addressed by SS F. The final switching signals are obtained with a look up table LUT addressed by SS F. The final switching state is determined by the redundant state selection RSS. The RSS changes the switching signals. The former one proposes a low switching frequency strategy for the RSS. This means that the RSS is only applied during the same QSWMI output voltage with redundant state S4 or S0 for evaluating the system performance. The principal characteristics of the PVGS are summarized in TABLE V.

The simulated PVGS used for PIS evaluation has 16 series connected photovoltaic cells (Shell SP150-P). It produces a maximum power point voltage of about 550V for the reference operation conditions of irradiance, 1000W/m², and temperature, 25°C, that satisfies the condition imposed in (24).

The irradiance profile selected to evaluate the PIS are shown in Fig. 12. This profile simulates the decreasing irradiance level when the sun is shadowed by a cloud. The irradiance changes presented in this profile are sharper than usual, so the PIS is evaluated in a harsher than normal conditions.

The PIS parameters values used in the simulation test and the grid voltage are shown in TABLE VI. Note the deviation of 10% that has been applied to C_i for evaluating the system performance in these conditions.

### TABLE V

<table>
<thead>
<tr>
<th>PVGS CHARACTERISTICS</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of series-parallel connected cells</td>
<td>16-1</td>
</tr>
<tr>
<td>Photovoltaic cell reference</td>
<td>SHELL SP150-P</td>
</tr>
<tr>
<td>Short-circuit current (25°C, 1000 W/m²)</td>
<td>4.8A</td>
</tr>
<tr>
<td>Open-circuit voltage (25°C, 1000 W/m²)</td>
<td>43.4V</td>
</tr>
<tr>
<td>MPP current (23°C, 1000 W/m²)</td>
<td>4.4A</td>
</tr>
<tr>
<td>MPP voltage (25°C, 1000 W/m²)</td>
<td>34V</td>
</tr>
</tbody>
</table>
The main magnitudes of the system when starting-up and when changing the irradiance conditions following the selected profile are shown in Fig. 13. As it can be seen in Fig. 13(a,b,c), the DC-Link capacitors are charged in the first part of the simulation by the photovoltaic cells without performing any control. The starting conditions reveal a disconnected PVGS so the photovoltaic cells are in open circuit. Then, the PIS is connected to the PVGS forcing it to a short circuit and the capacitors begin to get charged. Keeping in mind the curve of a photovoltaic cell, the PVGS current decreases until the capacitors are fully charged which set up the PVGS into an open circuit again.

Once the capacitors are charged at a minimum level, the PIS starts to operate with the control strategy exposed in previous chapters. The Fig. 13(c) shows how the MPP of the PVGS is tracked in the whole interval, including the zone with a sharply irradiance change.

In the charging interval, the capacitors reach a different level of voltage, Fig. 13(e,f), due to the different capacitance value of the two capacitors. This unbalance is rapidly reduced as soon as the PIS starts to control the system with its low frequency RSS control capability.

The capacitors voltage error, $v_{C,\text{error}} = v_{C2} - v_{C1}$, in the steady state is shown in Fig. 14. The two control strategies proposed for the RSS have been tested.

Obviously, the high switching frequency control (above 10kHz) presents less capacitor voltage errors, but it will produce higher losses which is not accord to the proposed system aim. In addition, this balancing strategy uses non-adjacent states of the full bridge which imply the switching of more than two switches at the same time.

The capacitor voltage balance at low switching frequency (to reduce switching losses) is enough to guarantee the correct performance of the overall system, and switches only between adjacent states.

### TABLE VI

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Grid voltage $V_s$</td>
<td>230V, 50Hz</td>
</tr>
<tr>
<td>Inductance $L_2$ (23) with $\alpha = 42^\circ$</td>
<td>100mH</td>
</tr>
<tr>
<td>Inductance $L_2$ (23) with $L_{Z_{\text{app}}}=2000$</td>
<td>100mH</td>
</tr>
<tr>
<td>Capacitor $C_2$ (30)</td>
<td>8mF</td>
</tr>
<tr>
<td>Capacitor $C_1$ (equal to $C_2$ with some deviation)</td>
<td>8.8mF</td>
</tr>
<tr>
<td>Switching frequency for HSFI</td>
<td>20kHz</td>
</tr>
</tbody>
</table>

Fig. 13. Main magnitude waveforms in the start-up process and with changing irradiance. (a) Power extracted from the PVGS. (b) PVGS Voltage. (c) PVGS Current. (d) RMS Supply reference current. (e) Capacitor 2 voltage. (f) Capacitor 1 voltage.

![Fig. 14. Capacitors voltage error: (a) with low frequency RSS and (b) with high frequency RSS.](image-url)
VI. PIS OPERATION ANALYSIS

The operation of the PIS has been evaluated in the steady state under two different irradiance conditions: 1000W/m² and 800W/m².

TABLE VII contains the value of all the important system variables under these conditions with the control strategy proposed. The 1000W/m² case takes the QSWMI to the optimal point of operation, where the triples and the quintuples harmonics are eliminated. The 800W/m² case takes the QSWMI to $Z_2$ where only the triples harmonics are zero. In both cases, the RSS control is set with low frequency.

A detail of the most representative waveforms for evaluating the PIS when the system has reached the steady state with 1000W/m² and 800W/m² are shown in Fig. 15 and Fig. 17 respectively.

The spectrum analyses of the main current waveforms in each case are shown in Fig. 16 and Fig. 18 (total harmonic distortion THD and individual harmonic distortion, $IHD_h$).

The QSWMI inverter generates a current that injects the power extracted from the PVGS (that matches the maximum power as shown in the previous section) into the grid. With 1000W/m² conditions, the quality of this current is quite good due to the fact that the multilevel operates in its optimal point ($THD < 5\%$ and all $IHD_h < 2\%$, Fig. 16(a)).

The HSFI performance maintains the total injected current quality and improves the harmonics with the highest content ($THD < 5\%$ and all $IHD_h < 0.5\%$, Fig. 16(c)).

However, with 800W/m² conditions, the QSWMI is not in the optimal situation (which is the most common case), and the quality of the current injected by him drops ($THD > 5\%$ and some $IHD_h > 4\%$, Fig. 18(a)). Here, the HSFI is justified, because improves the total injected current quality into an admissible value ($THD < 5\%$ and all $IHD_h < 1\%$, Fig. 18(c)).

The main advantage of the proposed system is the inverter loss decrease, because the QSWMI has low losses which are due principally to conduction. The switching losses are small because the switching frequency matches the grid frequency, near 50Hz, including the RSS control. The conduction losses could be even further reduced if a low ON-voltage semiconductor is selected, since no high speed switching semiconductors are needed for this inverter. The presence of the multilevel inverter improves the performance of the PIS if it is replaced by a two level inverter [5]. In addition, the multilevel can inject a higher amount of power into the grid.

![Figure 15](image1)

![Figure 16](image2)

**TABLE VII**

<table>
<thead>
<tr>
<th>Conditions</th>
<th>$V_{L1}$ (V)</th>
<th>$I_{L1}$ (A)</th>
<th>$V_{V1}$ (V)</th>
<th>$I_{V1}$ (A)</th>
<th>$\alpha$ (°)</th>
<th>$\beta$ (°)</th>
<th>Zone</th>
</tr>
</thead>
<tbody>
<tr>
<td>1000W/m²</td>
<td>403.4</td>
<td>10.4</td>
<td>544</td>
<td>4.4</td>
<td>42</td>
<td>38</td>
<td>$Z_1$</td>
</tr>
<tr>
<td>800W/m²</td>
<td>349.4</td>
<td>8.3</td>
<td>540</td>
<td>3.5</td>
<td>26</td>
<td>60</td>
<td>$Z_2$</td>
</tr>
</tbody>
</table>

But also the losses in the HSFI (principally due to the switching losses) decrease notably, because the current levels for this inverter are lower than those produced if it was working alone (without the QSWMI cooperation). This can be observed in Fig. 16(c), where the maximum instantaneous current value is lower than 1A, a value that is significantly lower than the maximum value of 13A for the total injected current, Fig. 16(a).

If one assumes that the switching losses are proportional to the maximum instantaneous current value, these losses will be reduced to approximately 8%. Therefore the high switching semiconductors used in this inverter will have a current ratio of about 13 times lower than the semiconductor used in a conventional PWM inverter for the same task. The reduction in losses allows one to use a smaller aluminum radiator. If the QSWMI is replaced by a two level inverter, the HSFI losses are higher [5].
of the current (this inductors are about 30% less expensive than air core inductors [18]), possibility of using slower semiconductors (so cheaper devices) for the greater current fraction, and using lower rating high frequency semiconductors (because they operate with a lower current fraction).

VII. CONCLUSIONS

In this paper a new topology for the power injection system used in photovoltaic generation systems is presented. This topology is based on the cooperative parallel association of two inverters, one is a three-level inverter operating at a low switching frequency (equal to the grid frequency) and the other at a usual VSI with standard switching frequency (above 10kHz) using a synchronous hysteresis controller. The performance of the proposed system was tested by simulation. The proposed system optimizes the system design, permitting the reduction of the system losses (conduction and switching losses, and Joule effect losses in inductors) and so increases the energy effectively injected into the grid. There will consequently be an increase in profit when selling this energy.

As the proposed system includes a multilevel inverter, two capacitor voltage balance strategies has been simulated, concluding that the low switching frequency one is better because reduce the overall switching losses, which is one of the main objectives of the proposed system. The resulting control system complexity is not excessive, because it could be said that the QSWMI is operated in a quasi-open-loop while the RSS is based on a logic table.

This paper’s results could be improved by substituting the hysteresis current controller used in the HSFI for another kind of high switching frequency current controller (for example, dead-beat current controller [14]) but it would result in a more complex control algorithm.

The authors are working at present on building a higher rating PIS prototype and evaluating the possibility to use high power semiconductors (like GTOs [19]) in the QSWMI. Also three-phase topologies are being developed.

ACKNOWLEDGMENTS

This research was supported by the Spanish Ministry of Education and Science, Code: ENE2006-10806/CON.

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